CLAIMS

1. A semiconductor apparatus formed on a semiconductor substrate having a first conductivity type, comprising:

an internal circuit in the central portion of said semiconductor substrate;

a plurality of external connection terminals formed in a first portion of said semiconductor substrate around said internal circuit, each external connection terminal being electrically connected to said internal circuit, wherein a plurality of power supplies correspondingly supply different voltage levels to the plurality of external connection terminals; and

a plurality of outer ESD protective circuits formed in a second portion of said semiconductor substrate or a common well region in said semiconductor substrate, around said first portion of said semiconductor substrate;

wherein each of said outer ESD protective circuits further comprises

a first diffusion region electrically connected to one of the external connection terminals,

a second diffusion region formed separately from said first diffusion region, said second diffusion region being electrically connected to a higher voltage line of a main power supply, and

a third diffusion region formed separately from said first diffusion region, at a side of said first diffusion region opposite from said second diffusion region, said third diffusion region being electrically

connected to a lower voltage line of said main power supply.

2. The semiconductor apparatus as claimed in claim 1, further comprising:

a first metal wiring formed in said second portion of said semiconductor substrate, wherein said first metal wiring electrically connects the second diffusion region of the plurality of outer ESD protective circuits to said higher voltage line of said main power supply; and

a second metal wiring formed in said second portion of said semiconductor substrate, wherein said second metal wiring electrically connects the third diffusion region of the plurality of outer ESD protective circuits to said lower voltage line of said main power supply.

3. The semiconductor apparatus claimed in claim 1, further comprising:

an oxide layer formed on a surface of said semiconductor substrate separating said first diffusion region from said second diffusion region and said first diffusion region from said third diffusion region;

a first electrode formed on said oxide layer between said first diffusion region and said second diffusion region; and

a second electrode formed on said oxide layer between said first diffusion region and said third diffusion region.

4. The semiconductor apparatus as claimed in claim 1, wherein said first diffusion region, said second diffusion region, and said third diffusion region are single-layered diffusion regions having a second conductivity type.

5. The semiconductor apparatus as claimed in claim 1, further comprising:

one or more extra outer ESD protective circuits corresponding to each external connection terminal formed in said second portion of said semiconductor substrate and said common well region in said semiconductor substrate or in an extra common well region separately formed around said second portion of said semiconductor substrate, the extra outer ESD protective circuits having substantially the same structure as the outer ESD protective circuit;

wherein

a second diffusion region of the extra outer ESD protective circuit is electrically connected to a higher voltage line of a power supply other than said main power supply; and

a third diffusion region of the extra outer ESD protective circuit is electrically connected to a lower

voltage line of said power supply other than said main power supply.

6. The semiconductor apparatus as claimed in claim 5, including a plurality of the extra outer ESD protective circuits corresponding to all power supplies.

7. The semiconductor apparatus as claimed in claim 5, wherein

the lower voltage of at least two power supplies is the ground voltage level; and

the extra outer ESD protective circuits corresponding to said at least two power supplies share the same third diffusion region electrically connected to the ground voltage level.

8. The semiconductor apparatus as claimed as claim 1, further comprising:

a plurality of inner ESD protective circuits on signal lines between said internal circuit and the plurality of external connection terminals, each inner ESD protective circuit being provided with a protective diode formed by a punch-through transistor having the same structure as a MOSFET formed in said internal circuit,

wherein a drain of said punch-through transistor is electrically connected to the signal line and a gate and a source of said punch-through transistor are electrically connected to a higher voltage line of a power supply corresponding to the external connection terminal or said main power supply.